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ANNEXES 1 to 7

**ANNEXES**

**to the**

**PROPOSAL FOR A REGULATION OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL**

**on a framework of measures for strengthening Europe's semiconductor ecosystem, repealing Regulation (EU) 2023/1781 (Chips Act 2.0)**

{SEC(2026) 504 final} - {SWD(2026) 504 final} - {SWD(2026) 505 final}

# ANNEX I Actions under the Chips for Europe Initiative 2.0

*Technical description of the Chips for Europe Initiative 2.0: scope of actions*

Where appropriate, the actions supported by the Chips for Europe Initiative 2.0 shall be implemented in accordance with the following technical descriptions:

## 1. Design capacities for integrated semiconductor technologies

*Context*

The Chips for Europe Initiative 2.0 shall support large-scale innovative design capacities for semiconductor technologies through a cloud-based design platform available across the Union. The design platform shall consist of innovative design facilities with extended libraries and tools, integrating a large number of existing and new technologies, including emerging technologies such as integrated photonics, quantum, and AI/neuromorphic. In combination with existing Electronic Design Automation tools, it shall allow the design of innovative components and new system concepts, and it demonstrates key functionalities, such as new approaches to high-performance, low-energy, security, new 3D and heterogeneous system architectures.

As the strategic backbone of the Chips for Europe Initiative 2.0, the platform shall provide a one-stop entry point, guiding users from design to prototyping and manufacturing, and uniting research, education, and industry. Its ultimate goal shall be to foster a new generation of Union fabless start-ups. Those companies contribute to developing innovative chips for Union user industries, capture the highest value in the semiconductor value chain, drive innovation in fast-growing markets, and reduce the Union's dependence on foreign design ecosystems.

*Status*

As of May 2026, a wide range of actors has been involved, including a Platform Coordination Team (PCT)[1], Design Enablement Teams[2], cloud providers, Electronic Design Automation (EDA) vendors, and IP providers. The design platform shall be implemented in a sequential manner: a Platform Coordination Team was first selected and put in place to operate the platform, host the central cloud infrastructure and coordinate user support services. The Design Enablement Teams have also been selected to provide tailored, end-to-end support for users throughout the chip development process. A contractor was selected for the central cloud infrastructure, which will host IP, pilot line Process Design Kits, and open-source EDA tools.

Negotiations are ongoing to select and onboard major EDA tool providers. These negotiations are expected to be concluded by autumn 2026. The first full-scale facilities are expected to become operational by end 2026.

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[1] The Platform Coordination Teams serves as the hosting entity for the Design Platform's virtual infrastructure and central services, coordinates access to a wide range of tools, assets and services, and assists the Chips JU in procuring the cloud platform.

[2] Design enablement teams assist users in setting up and customising design environments and flows, and to deploy Electronic Design Automation tools on the cloud.

The Design Platform shall be complemented by other actions to cultivate design related competences in the Union. This includes administering grants for start-ups and SMEs using the platform, support for open-source EDA tools development, and for the EuroPractice services that provide over 600 European universities with access to EDA tools for training at nominal costs as well as access to fabrication from leading foundries.

*Future outlook*

The Design Platform shall be continuously upgraded with new design capabilities as it continuously integrates more and more technologies and designs. This may include new open-source processor architectures and other innovative architectures, chiplets, programmable chips, new types of memory, processors, accelerators or low power chips.

The platform shall also integrate photonics and quantum chips IP, libraries and design automation tools in a fully integrated system approach (see also points 3 and 5 below). It shall also integrate the Process Design Kits (PDKs) of the main pilot lines of the Chips for Europe Initiative 2.0, as well as PDKs of industrial manufacturing facilities (subject to their prior agreement) in order to facilitate designing chips ready to be taped out in such pilot lines and industrial facilities.

The platform shall offer its services via the cloud, maximising access and openness to the whole community by networking existing and new design centres across the Member States. In particular, the platform shall offer support to startups, scaleups, and SMEs. It shall enlarge the Union's semiconductor ecosystem by integrating with different market sectors, such as health, mobility, energy, telecommunications, security, defence and space. More attention shall be given to industrialisation of innovative components designed on the platform and introduced on lead sectors.

## 2. Pilot lines for preparing for innovative production, testing and validation

*Context*

The Chips for Europe Initiative 2.0 shall support pilot lines for production, testing and validation bridging the gap from the lab to the fab of advanced semiconductor technologies, such as architectures and materials for power electronics, neuromorphic and embedded AI chips, integrated photonics, graphene and other 2D-material-based technologies, integrating electronics and microfluidics in heterogeneous systems.

*Status*

As of May 2026, five pilot lines are operational to varying extents, while more equipment, machinery, and tools are being added to increase the capability and capacity of the pilot lines. The pilot line technology areas were chosen to close the Union's most critical semiconductor gaps while building on existing strengths, securing long-term competitiveness, security of supply, and industrial resilience. The five pilot lines are the following:

- *sub-2 nm logic* anchors the Union in the advanced nodes that power AI, HPC, data centres and next-generation communications;
- *FD-SOI* capitalises on a field where the Union already leads, delivering low-power, high-reliability chips for automotive, mobility, industrial automation, and Internet of Things;

- *advanced packaging and heterogeneous integration* follow the observation that future performance gains hinge on system-level integration; the Union faces a strategic weakness in packaging but also a major opportunity to lead in chiplets, 3D stacking, and the co-integration of logic, memory, sensing, and connectivity;
- *wide-bandgap materials* (such as SiC and GaN) match the Union's strengths in power electronics and are vital for the energy transition, electric mobility, renewable infrastructure, and high-efficiency industrial systems; and
- *photonic integrated circuits*, which are increasingly important for high-bandwidth, low-power data transmission, sensing and advanced computing architectures in telecoms and data centres.

Moreover, 'Lab to Fab Accelerators' aim to achieve a rapid uptake by EU industry of the technologies developed under the pilot lines, in particular technologies related to advanced packaging and heterogeneous integration.

*Future outlook*

Pilot lines shall continue to support experimentation, test, and validation, including through Process Design Kits (PDKs), of the performance of IP blocks, virtual prototypes, new designs and novel integrated heterogeneous systems in an open and accessible way. Their PDKs shall be integrated in the design platform in order to enable access for design and (virtual) prototyping projects.

Current pilot lines shall increasingly focus on industrialisation and deployment of pilot line technologies to support the Union's semiconductor ecosystem.

New or upgraded pilot lines may be supported for emerging challenges, such as energy efficient AI chips; leading edge technologies such as CFET devices and monolithic 3D integrated circuits for higher performance and lower power consumption; ferroelectric, resistive and charge based memories enabling ultra-fast and ultra-low power operations.

Furthermore, new or upgraded pilot testbeds may be supported where different innovative technologies or products are combined and integrated for the development and validation of new devices in key applications and user industries. An example is a testbed for the miniaturisation, advanced optics, and laser projection technologies related to smart glasses. Pilot testbeds shall help identify risks, validate performance, and ensure feasibility in real-world conditions before full industrial-scale deployment.

## 3. Advanced technology and engineering capacities for quantum chips

*Context*

The Chips for Europe Initiative 2.0 shall support the development of quantum chips and associated technologies, including those based on semiconductor material or integrated with photonics. Dedicated actions shall include design libraries for quantum chips, pilot lines for building quantum chips, and facilities for testing and validating quantum chips produced by the pilot lines. The aim is to provide Union researchers, start-ups and industry with reliable access to facilities capable of producing and validating the main quantum chip technologies.

*Status*

As of May 2026, six quantum chip pilot lines are established, one for each of the leading Union technology platforms: superconducting, spin, photonic, diamond, neutral-atom, and

trapped-ion chips. The projects focus on setting up stable pilot-scale fabrication processes, integrating testing and experimentation facilities, developing early industrialisation roadmaps, and laying the groundwork for future scaling.

| Pilot line | Name | Coordinator |
|---|---|---|
| Superconducting | SUPREME | VTT (FI) |
| Spin | SPINS | IMEC (BE) |
| Photonic | P4Q | University of Twente (NL) |
| Diamond | DIREQT | CNR (IT) |
| Neutral atoms | Q-PLANET | PASCAL (FR) |
| Trapped ion | CHAMP-ION | SAL (AT) |

In addition, activities shall be addressed to support the emergence of a pan-European quantum design community around quantum chip design, simulation, and verification libraries and tools. Finally, enabling technologies shall be supported, including the electronics, cryogenics, packaging and interfacing subsystems that prepare, protect, control, interconnect, and read-out core quantum devices.

*Future outlook*

Advanced technology and engineering capacities for quantum chips shall continue to be built out and enhanced. This includes design capabilities, design libraries for quantum chips, pilot lines, testing and experimentation facilities, enabling technologies. Support to first industrialisation efforts of the most mature developments shall also be provided. A differentiation in support shall be made for different technology platforms. Maturation of quantum chip technologies shall lead to increased industrialisation.

## 4. A network of semiconductor competence centres and skills development

*Context*

The Chips for Europe Initiative 2.0 shall support the operation of a network of semiconductor competence centres. These centres shall provide structured access to technical expertise, testing facilities, and advisory services, and enable companies (particularly SMEs and start-ups) to strengthen their design capabilities, experiment with new technologies, and develop specialised skills. Competence centres shall play a key role in addressing the Union's skills gap in semiconductor technologies.

*Status*

As of May 2026, competence centres have been established in all Member States, as well as in Norway. In addition, a support action was defined to set up and coordinate the work of the national competence centres. The support action has launched a Training and Skills Development focus group which drives collaboration among the competence centres to roll

out education and upskilling initiatives, to create training concepts, and to provide specific training and access to the design platform and pilot lines.

*Future outlook*

Semiconductor competence centres shall continue to be supported. The possibility to launch new centres or to refocus existing centres depending on market and technology developments shall be analysed. The cooperation between competence centres in the overall network shall be strengthened, where possible. Furthermore, the support by competence centres on skills development shall be enhanced, including by fostering cooperation with higher education and vocational training providers, by collaborating closely with the Pact for Skills and the skills working group of the Industrial Alliance, and by increasing the visibility and attractiveness of the semiconductor sector.

## 5. Advanced design, prototyping, and industrial deployment capacities for photonic integrated circuit technologies

*Context*

This new component of the Chips for Europe Initiative supports the development of photonic integrated circuits and associated technologies. Actions include developing design libraries and design automation tools for photonic integrated circuits and enhancing existing and/or setting up new pilot lines for the prototyping and production of photonic integrated circuits. Capabilities in production technologies including co-packaging and heterogeneous integration with electronic chips, manufacturing equipment, and materials platforms for photonic integrated circuits shall be strengthened.

*Status*

As of May 2026, a pilot line on photonic integrated circuits has been inaugurated. This pilot line offers open-access fabrication services across 14 hosting sites, covering multiple photonic material platforms from silicon and silicon nitride to indium phosphide. Services include chip fabrication runs, hybrid integration, packaging, testing, and reliability qualification. Technology demonstrators are planned, including co-packaged optics for AI data centres, LiDAR sensors, visible light engines for AR/VR, and programmable photonic processors. Furthermore, apart from the pilot line, industrial-grade demonstrators of advanced photonic technologies are developed that need to show scalability, reliability, and integration-readiness.

*Future outlook*

Photonic integrated circuits and associated technologies shall continue to be supported. This shall include design tools, design libraries, pilot lines, demonstrators, training services. Specific attention shall be dedicated to the transfer and industrial uptake of technologies developed under this component of the Chips for Europe Initiative 2.0.

## 6. Chips Fund activities for access to capital by start-ups, scale-ups, and SMEs

*Context*

The Chips for Europe Initiative 2.0 shall support the creation of a thriving semiconductor and quantum innovation ecosystem by supporting access to venture capital for start-ups, scale-ups and SMEs to grow their business and expand their market presence in a sustainable manner.

*Status*

As of May 2026, the Chips Fund is implemented through two thematic investment facilities: the European Innovation Council's Accelerator programme, with Horizon Europe funding in blended grant and equity for high-risk, deep-tech startups; and the InvestEU Fund, managed by the European Investment Fund, with a guarantee from the Digital Europe Programme, for intermediated equity investments ranging from seed to growth stage. The EUR 300 million available budget for the Accelerator programme was fully deployed in just two years and supports 24 highly innovative startups with a total of EUR 62 million in grants and EUR 238 million in recommended equity investment. On the InvestEU leg of the Chips Fund, four financial partners have been selected and EUR 68 million in funds have been signed or approved with them, resulting so far in 31 companies from early to growth stage having received EUR 116 million equity investment.

*Future outlook*

Whereas attention for startups shall continue, more focus shall be put on scaleups and later stage funding. Considerable funding from the Scaleup Europe Fund for deep-tech scaleups shall be increasingly deployed, leveraging additional private venture capital.

## 7. Grand challenges

*Context*

This new component of the Chips for Europe Initiative 2.0 shall support large-scale, cross-sectoral initiatives addressing major technological and industrial challenges of strategic relevance for the Union ('grand challenges'), which potentially affect different ecosystems. Grand challenges are expected to result in technology advances in mainstream and leading-edge technologies, end-to-end product integration through the whole product development lifecycle, and their pre-commercial industrialisation.

*Status*

As of May 2026, no prior activities have been carried out under the banner of 'grand challenges' under the Initiative.

*Future outlook*

Possible grand challenges that can be targeted may include the development of new computing technologies for drastic (say times 1000) energy reduction. The grand challenge would result in energy-efficient, secure and distributed AI infrastructures, enabling high-performance AI accelerators (HBM-class memory, stacked logic, optical/RF interconnects), agentic/embodied AI systems, contextual edge intelligence and secure low-power infrastructures. The development of energy-efficient chips, including AI chips, shall also support the grand challenge "pioneering energy- and resource-efficient compute infrastructure, with a view to enhancing their sustainability at scale" as identified under the Cloud and AI Development Act (CADA)[3]. A close link between the R&I activities to address the two complementary challenges shall be established, including possible coordinated calls for proposals.

Another grand challenge shall be the development of processors and accelerators, which are designed and, where appropriate, manufactured in the EU, and that would become part of a cloud and AI stack. This grand challenge shall again be closely linked and contribute to a

[3] See Article 4 of the Cloud and AI Development Act

CADA grand challenge, namely 'reaching autonomy across the cloud and AI stack, with a view to eliminate dependencies in critical technologies' [4]. The grand challenge may target in particular solutions developed by upcoming startups and may include the use of innovation procurement. Again, a close link between the R&I activities to address the two complementary challenges shall be established, including possible coordinated calls for proposals.

A third grand challenge may be in physical AI, to provide the foundational technologies to enable a wide range of future applications, services, and autonomous systems from, for example, humanoid to industrial robots and their deployment, in particular, in med-tech and healthcare to manufacturing, aerospace and defence. R&I in physical AI shall lead to advances in mainstream technologies such as power semiconductors, microcontrollers, and analog-/mixed signal- and sensor technologies. R&I shall be followed by industrial production and commercialisation of embedded advanced AI into autonomous machines, robots, broadband networks, and next-generation connected devices.

A fourth grand challenge may be on smart glasses and virtual worlds. A recent Commission Communication sets out the strategy and proposed actions on virtual worlds and Web 4.0[5]. In this context, optics, photonics and semiconductor technologies are crucial for realizing sensing and visualization devices supporting Virtual Worlds applications such as smart glasses. R&I shall significantly improve the quality, performance, and efficiency of processing and communicating Virtual Worlds content. A grand challenge for smart glasses shall aim at integrating relevant ultra-low power components, such as power electronics, sensors, cameras, audio devices, lasers, specialty glasses, displays, neuromorphic or AI chips into working prototypes and demonstrators.

Grand challenges may address market targets as well, for example, taping out chips from 100 fabless startups including 10 unicorns by 2035. Another type of grand challenges may address lead markets and demand stimulation, for example, by developing automotive hardware platforms or the full stack for AI (Giga) Factories. Grand challenges may also address new semiconductor production technologies, for instance increasing recycling and boosting circularity of materials, or the development of advanced semiconductors cooling technologies.

Industrialisation of new technologies shall be an essential part of the grand challenges.

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4 See Article 5 of the Cloud and AI Development Act

5 Communication from the Commission to the European Parliament, the Council, the European Economic and Social Committee and the Committee of the Regions, "An EU initiative on Web 4.0 and virtual worlds: a head start in the next technological", COM(2023) 442 final, 11 July 2023.

## Annex II Priority areas for strategic projects

*Technical description of potential priority areas for strategic projects: scope of actions*

### 1. European Advanced Semiconductor Manufacturing[6]

Reinforced action should be taken to create a sustained demand for advanced semiconductors through the development of the EU advanced technology ecosystem. EU sovereignty and supply security in the area of advanced chips production and innovation is essential to foster a thriving and competitive EU semiconductor ecosystem, with reduced reliance on foreign supply chains. This is particularly important to cater for the increased demand for AI and cloud infrastructure. In addition, advanced chips are indispensable for strategic industry sectors such as defence, health, space, robotics, healthcare, secure communications, drones, and autonomous vehicles. They are also critical inputs for emerging and high-value areas such as photonics and quantum chips.

This strategic project aims to establish an EU semiconductor plant that combines leading-edge node chip manufacturing with chiplet integration and 2.5D/3D packaging. It shall build on solid research foundations, which have been validated in the Chips for Europe Initiative under the Chips Act. The manufacturing facility shall adhere to European values, including guarantees for confidentiality, integrity and traceability of chips, in particular for sensitive and strategic applications and infrastructure. European companies could help create demand by offering growth incentives for fabless chips and AI-driven system design. Public and private investments are estimated between EUR 20 and 40 billion depending on the option chosen. EUR 3 to 4 billion public and private investments could be mobilised to foster the growth of fabless chip design companies across the EU through funding from under the next MFF, Member States, and relevant industries and private investors.

This project to be developed in close collaboration with domestic and international stakeholders, including credible technology and manufacturing partners, shall enable the establishment of cutting-edge capacities that reduce structural dependencies on non-EU suppliers, increase supply security for sectors such as AI, defence, space, healthcare, telecoms and automotive, and reinforce the EU's technological sovereignty.

As a first step, an informal call for expressions of interest may be launched. After analysis of submitted expressions, a call for proposals may follow.

### 2. AI chips and systems for EU compute infrastructure

The Union is currently dependent on foreign AI chips and integrated systems, resulting in significant capital outflow to import critical foreign AI technologies. Strengthening the Union's technological sovereignty therefore requires building competitive, home-grown capacity at chip level and across the entire compute stack.

This strategic project aims to design, develop, prototype, and tape-out AI chips and compute systems based on advanced European technologies. AI chip design shall result in the development of demonstrators and prototypes that can be evaluated on a common testbed against clear benchmarks. Full-rack AI system prototypes shall be developed, including AI accelerators, high bandwidth memory, boards, ultra-low-latency networking and full software

[6] This part expands on a potential implementation of Article 19.

stack, and shall be delivered for comparative evaluation on agreed workloads. Rack-level system prototypes shall be demonstrated on a common EU testbed. Final testing and scoring shall use clear KPIs on common EU testbeds operated by a neutral facility.

This strategic project shall reduce reliance on non-EU suppliers and increase technological sovereignty across the full AI stack. It shall strengthen the EU ecosystem for design, integration and optimisation of high-performance AI systems, with R&D activities, data handling and testing executed in the Union, thereby anchoring skills, know-how and supply chains in Europe. Take-up of the AI systems shall create further demand to justify further investments in manufacturing in Europe.

As a first step, an informal call for expressions of interest may be launched. After analysis of submitted expressions, a call for proposals may follow.

### 3. Automotive application processor for autonomous driving

The automotive industry is currently undergoing a pivotal transformation, primarily driven by the emergence of electric, connected, autonomous vehicles. This shift necessitates a more centralised, integrated, and flexible electrical/electronic (E/E) architecture to accommodate the advanced computing needs of autonomous driving systems, ensure seamless vehicle connectivity, support electric vehicle (EV) power management, and enable new mobility services. Currently, European automotive OEMs rely on non-European suppliers for the application processors that enable autonomous driving, which creates dependencies, possible vulnerabilities that can be exploited, as well as potential security risks.

This strategic project aims to design, develop, prototype, and tape-out high-performance RISC-V based automotive application processors. These processors shall include advanced computer architecture techniques, multi-core configurations and support for high-bandwidth memory interfaces, catering to the complex computing demands of autonomous driving systems. In addition, AI and ML accelerators shall be developed with specialised Instruction Set Architecture (ISA) extensions for efficient data-intensive computations. These accelerators shall be optimised for automotive applications, supporting advanced AI models with a focus on energy efficiency, reduced latency, and real-time processing capabilities. The end result shall be an industry-grade silicon tape-out, incorporating a competitive RISC-V application processor alongside memory, accelerators and any other relevant IP taking advantage of advanced packaging techniques. A mature toolset shall accompany the hardware development. Automotive companies shall be able to deploy the results in an operational environment as qualified devices.

The strategic project shall address Europe's technological sovereignty in automotive AI processors and accelerators. It shall reduce the dependence of European automotive OEMs on foreign suppliers. Take-up of the application processors and accelerators shall create further demand to justify further investments in manufacturing in Europe.

As a first step, an informal call for expressions of interest may be launched. After analysis of submitted expressions, a call for proposals may follow.

### 4. European memory fabrication facility

Memory chips, such as DRAM, NAND, and emerging non-volatile memories, are essential components in datacentres, AI systems, automotive electronics, telecommunications equipment, industrial automation, and defence applications. Currently, the global memory market is heavily concentrated in Asia (South Korea, Taiwan, China) and the United States.

The EU lacks indigenous memory production capacity, leaving critical European supply chains highly vulnerable to geopolitical shocks, trade disputes and natural disasters. This dependency has become critically apparent in 2026, as surging demand for AI-related high-bandwidth memory (HBM) has led manufacturers to reallocate production capacity away from standard DRAM and NAND, triggering price surges in some segments and severe allocation shortages for European industries. Hence, the absence of a European memory fab constitutes a strategic vulnerability for the EU's digital sovereignty, economic resilience and defence readiness. A strategic project for a European memory fab would be necessary not only to secure supply for key industries, but also to anchor advanced manufacturing know-how, stimulate innovation across the semiconductor value chain and support the EU's broader objectives under industrial, digital, and economic security policies.

The strategic project for the establishment of a European memory fabrication facility shall require a consortium-based approach, combining public funding from the EU and participating Member States with substantial private investment, likely in the range of EUR 15-30 billion given the capital intensity of modern memory fabs. A European-led joint venture could be considered to build a differentiated position, such as embedded memory, low-power memory, or emerging technologies linked to AI and edge computing. A phased approach may begin with a pilot/R&D line before scaling to high-volume manufacturing, mitigating risk and building capability incrementally.

A dedicated call for expressions of interest may be structured to identify industrial partners, technology providers, and Member State hosts willing to commit to this strategic initiative.

## 5. Leading-edge chip design

While building physical manufacturing facilities is vital, a large share of the economic value, profit margins, and technological control in the semiconductor supply chain lies in chip design, architecture, and intellectual property. Europe has important strengths in research, automotive semiconductors, and semiconductor equipment; however, it remains comparatively weak in the large-scale design of the most advanced logic chips, particularly those based on leading-edge architectures and process nodes. As a result, the EU relies heavily on non-European companies for advanced compute and AI capabilities. Without indigenous leading-edge design capacity, Europe risks remaining dependent on foreign architectures, leaving critical infrastructure, defence, and AI-related industries exposed to geopolitical restrictions, supply dependencies, and vendor lock-in. Strengthening chip design capabilities would allow the EU not only to capture more value within the semiconductor value chain, but also to embed European priorities such as security, privacy, resilience, and energy efficiency directly into advanced hardware.

A strategic project for leading-edge chip design shall aim to establish sovereign, world-class capability within the EU for the design of cutting-edge logic chips, focusing on intellectual property, architecture, and verification rather than manufacturing. Focus areas may include:

- Advanced AI accelerators for cloud, edge, and industrial applications (including for geospatial modelling and digital twins)
- High-performance processors for supercomputing and datacentres
- Secure-by-design chips for critical infrastructure, defence, aeronautics and space
- Domain-specific processors for autonomous vehicles, robotics, and industrial automation

- Application-Specific Integrated Circuits (ASICs) and System-on-Chips (SoCs) for 5G/6G telecommunications
- RISC-V-based open-architecture processors at leading-edge nodes
- Advanced chiplet platforms for 2.5D/3D integration across automotive, aerospace, and telecom applications

Implementation may take the form of a large-scale public-private partnership mobilising EUR 8-12 billion in combined EU, Member State, and private funding, structured around consortia centred around fabless semiconductor firms, and involving ASIC design houses, Electronic Design Automation tool vendors, IP providers, research institutes, and end-user industries (automotive and aeronautical Original Equipment Manufacturers, telecom operators, defence primes). Investment shall cover chip architecture and design teams, advanced design tools and IP libraries, prototyping, verification, software stacks, and industrialisation. The project shall have guaranteed access to advanced fabrication through partnerships with leading foundries or European pilot lines at 2nm and below. A phased approach may begin with capability mapping and target application selection, followed by design and validation programmes, pilot tape-outs, ecosystem development, and commercial deployment, alongside dedicated measures to develop talent and attract world-class engineering expertise.

A call for expression of interest may invite proposals from industrial consortia for leading-edge chip design projects with clear strategic relevance, asking applicants to specify the target application domain, expected technological differentiation, required investment, access to design and manufacturing infrastructure, timeline to prototype and commercialisation, and contribution to Europe's resilience and competitiveness.

## 6. Strengthening key segments of the value chain

The Union faces several vulnerabilities in the semiconductor value chain. Many of these vulnerabilities are well-known, including the ones above, whereas others are less obvious and/or considered less critical. The latter vulnerabilities may come to the surface when certain events take place, revealing their full impact and exposing dependencies, as witnessed in the Nexperia case (see Staff Working Document).

It will not be feasible or practical for the Union to address all possible vulnerabilities in the semiconductor value chain. However, it may be desirable for the Union to have the possibility to reduce some vulnerabilities and strengthen key segments of the value chain, especially when disruptions demonstrated dependencies or when such disruptions are likely to happen.

This type of strategic projects aims to strengthen a particular key segment of the semiconductor value chain. Such interventions shall not be limited to the most advanced parts of the value chain, and may address, for instance, the production of mainstream chips, back-end processes, Printed Circuit Board (PCB) assembly, and also materials and equipment. An example of a potential strategic project may be the setup of an OSAT[7] facility that would predominantly cater for European user industries. Another example may be the setup of an advanced packaging facility that would complement (new) front-end fabs. The main participants in strategic projects shall be companies headquartered in the Union, and prime investment shall typically, but not necessarily always, take place in the Union.

[7] OSATs – Outsourced Semiconductor Assembly and Test – are third-party service providers who specialise in the final, critical stages of chip manufacturing, i.e. packaging the semiconductor die and testing it for functionality before it reaches customers.

This type of strategic projects shall address suspected and proven vulnerabilities in the semiconductor value chain. Using targeted actions to strengthen key segments of the value chain shall increase Europe's technological sovereignty and reduce dependencies on foreign actors.

The European Semiconductor Board shall have a key role in selecting the areas of the value chain where strengthening is needed. As a next step, an informal call for expressions of interest may be launched. After analysis of submitted expressions, a call for proposals may follow.

## ANNEX III Measurable indicators to monitor the implementation and to report on the progress of this Regulation towards the achievement of its objectives

The Commission shall be responsible for monitoring the implementation of this Regulation on a regular basis, possibly with the support of external studies, Member State and market data. The Commission shall carry out a comprehensive evaluation of the effectiveness, efficiency, coherence, proportionality, and subsidiarity of this Regulation. **An evaluation report** presenting the main findings shall be submitted to the European Parliament, the Council, the European Economic and Social Committee, and the Committee of the Regions in line with Article 60 of this Regulation. Where appropriate, the Commission may accompany this report with proposals for improving or adapting this Regulation.

The Commission, in close cooperation with the Member States, shall regularly monitor the implementation and application of the legal provisions, with particular attention to the effectiveness of the adopted measures. Monitoring activities shall rely on quantitative and qualitative indicators, drawing from data provided by stakeholders across the semiconductor value chain, Member States, and relevant Union bodies.

The measurable indicators shall build on the two general objectives of this Regulation.

**General monitoring indicators:**

- total semiconductor related FDI inflows into the Union;
- skilled workforce in semiconductor and photonics, including workforce trained/reskilled through the national chips competence centres' initiatives;
- public support to start-ups and scale ups; and
- scale-up funding via private equity and Venture Capital.

**Specific monitoring indicators:**

First specific monitoring indicators for enhancing the capacity, security of supply and competitiveness of the EU semiconductor industry across the value chain, including for leading-edge AI chips:

- Union share of global semiconductor value (in EUR) in the different segments of the value chain:
    - design, IP, EDA;
    - manufacturing;
    - equipment manufacturing;
    - OSAT (Packaging);
    - materials / gases;
- top Union firms in any value chain segment;
- installed wafer fabrication capacity in the Union (wpm).

Second specific monitoring indicator for developing a strong user market across key industry sectors: Consumption of chips by key sectors (automotive, energy, health, defence, telecom, AI/data centres/cloud) in value (EUR).

Third specific monitoring indicator for increasing intelligence capabilities for crisis preparedness and response: Coverage (in %) of the Union semiconductor value chain monitored by the Business-to-Business Semiconductor Supply Chain Platform.

## ANNEX IV Synergies of this Regulation with other programmes

(1) Synergies of the Chips for Europe Initiative 2.0 with the Specific Objectives 1 to 5 of the **Digital Europe Programme** shall ensure that:

(a) the targeted thematic focus of the Chips for Europe Initiative 2.0 on semiconductor and quantum technologies is complementary;

(b) Specific Objectives 1 to 5 of the Digital Europe Programme support digital capacity building in the advanced digital technologies, including High Performance Computing, AI and cybersecurity, and advanced digital skills;

(c) The Chips for Europe Initiative 2.0 will invest in capacity building to reinforce advanced design, production and systems integration capabilities in cutting-edge semiconductor technologies, next-generation semiconductor technologies and cutting-edge quantum technologies for innovative business development, strengthening the Union's semiconductor supply and value chains, serving key industrial sectors and creating new markets.

(2) Synergies with **Horizon Europe** shall ensure that:

(a) although thematic areas addressed by the Chips for Europe Initiative 2.0 and several areas of Horizon Europe converge, the type of actions to be supported, their expected outputs and their intervention logic are different and complementary;

(b) Horizon Europe provides extensive support for research, technological development, demonstration, piloting, proof-of-concept, testing and prototyping, including pre-commercial deployment of innovative digital technologies, in particular through:

(i) a dedicated budget in the pillar 'Global Challenges and European Industrial Competitiveness' for the cluster 'Digital, Industry and Space' to develop enabling technologies (AI and robotics, Next Generation internet, High Performance Computing and Big Data, key digital technologies (incl. microelectronics), combining digital with other technologies);

(ii) support to research infrastructures under the pillar 'Excellent Science';

(iii) the integration of digital across all the Global Challenges (health, security, energy and mobility, climate, etc.); and

(iv) support for scale-up breakthrough innovations under the pillar 'Innovative Europe' (many of which will combine digital and other technologies).

(c) the Chips for Europe Initiative 2.0 is exclusively focusing on building large-scale capacities in semiconductor and quantum technologies across the Union. It will invest in:

(i) fostering innovation by supporting two closely interlinked technological capacities that enable designing novel system concepts and their testing and validation in pilot lines;

(ii) providing targeted support to build training capacity and enhance applied advanced digital competences and skills to support development and

deployment of semiconductors by technology development and end-user industries; and

(iii) a network of national competence centres, which facilitate access and provide expertise and innovation services to end-user communities and industries, to develop new products and applications and to address market failures.

(d) the technology capacities of the Chips for Europe Initiative 2.0 will be made available to the research and innovation community, including for actions supported through Horizon Europe;

(e) as the development of novel digital technologies in the area of semiconductors matures through Horizon Europe, those technologies where possible progressively will be taken up and deployed by the Chips for Europe Initiative 2.0;

(f) the Horizon Europe programmes established under Regulation (EU) 2021/695 for the development of skills and competencies curricula, including those delivered at the co-location centres of the European Institute of Innovation & Technology's Knowledge and Innovation Communities, are complemented by capacity building in advanced applied digital skills and competences in semiconductor and quantum technologies supported by the Chips for Europe Initiative 2.0;

(g) strong coordination mechanisms for programming and implementation are put in place, aligning all procedures for both Horizon Europe and the Chips for Europe Initiative 2.0 to the extent possible; their governance structures will involve all Commission services concerned.

(3) Synergies with the proposed **Cloud and AI Development Act (CADA)** shall contribute to a coherent approach to strengthening the Union's technological sovereignty, by addressing both the supply of and demand for advanced semiconductor technologies, in particular through:

(a) leveraging demand for semiconductors stemming from cloud and AI development: this Regulation shall support the capacity of the Union to respond to the demand of high-performance and energy-efficient semiconductors generated by the expansion of cloud and AI infrastructure, including data centres and large-scale computing facilities;

(b) supporting the deployment of AI Factories and AI Gigafactories: this Regulation shall support the availability of advanced and specialised semiconductors required for high-performance computing and artificial intelligence applications, thereby enabling the deployment and scaling of AI Factories and AI Gigafactories in the Union and contributing to industrial-scale AI development and scientific capabilities.

(c) supporting secure and resilient digital infrastructures: this Regulation shall contribute to ensuring the availability of components needed for the development of trusted and sovereign cloud and AI environments for critical use cases needed to increase reliance on secure and reliable hardware components by strengthening the resilience and security of semiconductor value chains.

(d) supporting the deployment of digital infrastructures based on Union technological capabilities and reduce exposure to external dependencies;

(e) contributing to sustainability objectives of digital infrastructure deployment: this Regulation shall support the development and production of resource-efficient and energy-efficient semiconductors in order to address the growing deployment of data centres and cloud infrastructure which is expected to increase demand for energy-efficient digital technologies;

(4) Synergies with Union programmes under shared management, including **the European Regional Development Fund, the European Social Fund Plus, the European Agricultural Fund for Rural Development and the European Maritime, Fisheries and Aquaculture Fund**, shall ensure the development and strengthening of regional and local innovation ecosystems, industrial transformation, as well as the digital transformation of society and of public administrations. This includes support for the digital transformation of industry and the take-up of results, as well as the rolling out of novel technologies and innovative solutions. The Chips for Europe Initiative 2.0 will complement and support the transnational networking and mapping of capacities it will support and make them accessible to SMEs and end-user industries in all Union regions.

(5) Synergies with the **Connecting Europe Facility** shall ensure that:

(a) the Chips for Europe Initiative 2.0 focuses on large-scale digital capacity and infrastructure building in the areas of semiconductors aiming at the wide uptake and deployment across the Union of critical existing or tested innovative digital solutions within a Union framework in areas of public interest or market failure. The Chips for Europe Initiative 2.0 is mainly to be implemented through coordinated and strategic investments with Member States, in building digital capacities in semiconductor technologies to be shared across the Union and in Union-wide actions. This is particularly relevant in electrification and autonomous driving, and is intended to benefit and facilitate the development of more competitive end-use industries, particularly in the mobility and transport sectors;

(b) the capacities and infrastructures of the Chips for Europe Initiative 2.0 are to be made available to testing of innovative new technologies and solutions that can be taken up in the mobility and transport industries. The Connecting Europe Facility is to support the roll-out and deployment of innovative new technologies and solutions in the field of mobility and transport as well as in other domains;

(c) coordination mechanisms are to be established, in particular through appropriate governance structures.

(6) Synergies with **InvestEU Programme** shall ensure that:

(a) support through market-based financing, including pursuing policy objectives under the Chips for Europe Initiative 2.0 is provided by Regulation (EU) 2021/523; such market-based financing might be combined with the grant support;

(b) a blending facility under the InvestEU Fund is supported by financing provided by Horizon Europe or the Digital Europe Programme in the form of financial instruments within blending operations.

(7) Synergies with **Erasmus+** shall ensure that:

(a) the Chips for Europe Initiative 2.0 supports the development and acquisition of the advanced digital skills needed for the development and deployment of cutting-edge semiconductor technologies in cooperation with relevant industries;

(b) the advanced skills part of Erasmus+ complements the interventions of the Chips for Europe Initiative 2.0, addressing the acquisition of skills in all domains and at all levels through mobility experiences.

(8) Synergies with other **Union programmes and initiatives on competencies and skills** shall be ensured.

(9) Synergies with **Union cybersecurity legislation** shall ensure that:

(a) investments supported under the Chips for Europe Initiative 2.0 contribute to strengthening the security and resilience of semiconductor supply chains in the Union;

(b) the Chips for Europe Initiative 2.0 complements the objectives of the Cyber Resilience Act and the EU Cybersecurity Act by supporting the development and deployment of trusted semiconductor technologies;

(c) coordination is ensured with the implementation of Directive (EU) 2022/2555 (Network and Information Security Directive, NIS2), including where appropriate the promotion of trusted chips in critical sectors.

(10) Synergies with **Important Projects of Common European Interest (IPCEIs) and relevant State aid frameworks** shall ensure that:

(a) actions supported under the Chips for Europe Initiative 2.0 remain coherent with existing State aid and competition rules, including the R&D&I Framework and the IPCEI Communication;

(b) IPCEIs, including the IPCEI candidate on Advanced Semiconductor Technologies (AST), may contribute to bridging research and innovation activities with industrial deployment and manufacturing capacities, thereby complementing the objectives of the Chips for Europe Initiative 2.0;

(c) the Chips for Europe Initiative 2.0 addresses complementary investment gaps to the support of first-of-a-kind semiconductor manufacturing facilities and related technological capacities.

(11) Synergies with **national semiconductor strategies, roadmaps and investment plans** shall ensure that:

(a) Member States' national semiconductor strategies and investment plans are aligned with the objectives of the Chips for Europe Initiative 2.0;

(b) national and Union investments contribute to strengthening regional and cross-border semiconductor ecosystems across the Union;

(c) coordination mechanisms support the mapping of semiconductor capacities and facilitate cooperation between Member States in order to strengthen the resilience of the Union's semiconductor value chains and avoid unnecessary duplication of investments.

## ANNEX V Critical Sectors

(1) Energy
(2) Transport
(3) Banking
(4) Financial market infrastructure
(5) Health
(6) Drinking water
(7) Waste water
(8) Digital infrastructure
(9) Public administration
(10) Space
(11) Production, processing and distribution of food
(12) Defence
(13) Security

## ANNEX VI Industrial sectors using semiconductors

(1) Automotive

(2) Datacentres, cloud and AI

(3) Industrial automation and robotics

(4) Aeronautics

(5) Space, defence and security

(6) Electronic communications infrastructures

(7) Industrial-grade computing and IoT

(8) Health care and medical devices

(9) Electronic manufacturing services providers and distributors

(10) Renewable and low carbon energy systems

## ANNEX VII Correlation table

| Regulation 2023/1781 | This Regulation |
|---|---|
| Article 1 | Article 1 |
| Article 2 | Article 2 |
| Article 3 | Article 3 |
| Article 4 | Article 4 |
| Article 5 | Article 5 |
| Article 6 | Article 11 |
| Article 7 | - |
| Article 8 | - |
| Article 9 | - |
| Article 10 | - |
| Article 11 | Article 6 |
| Article 12 | Article 12 |
| Articles 13 to 14 | Article 14 |
| Article 15 | Article 15 |
| Article 16 | Article 13 |
| Article 17 | - |
| Article 18 | Article 21 |
| Article 19 | Article 33 |
| Article 20 | Article 35 |

| | |
|---|---|
| Article 21 | Article 36 |
| Article 22 | Article 37 |
| Article 23 | Article 39 |
| Article 24 | Article 40 |
| Article 25 | Article 41 |
| Article 26 | Article 42 |
| Article 27 | Article 43 |
| Article 28 | Article 44 |
| Article 29 | Article 45 |
| Article 30 | Article 46 |
| Article 31 | Article 48 |
| Article 32 | Article 50 |
| Article 33 | Article 51 |
| Article 34 | Article 52 |
| Article 35 | Article 53 |
| Article 36 | Article 54 |
| Article 37 | Article 55 |
| Article 38 | Article 56 |
| Article 39 | - |
| Article 40 | Article 57 |
| Article 41 | Article 60 |